

Claims:

1           1.       A power management system for a computer system having one or more different  
2 components wherein power is dynamically supplied to each component, the power management  
3 system comprising:

4               a clock generator circuit for generating one or more different clock signals wherein each  
5 clock signal has a different predetermined frequency;

6               a clock selector circuit that, based on the task being performed by the computer system,  
7 dynamically adjusts the clock signal supplied to each component of the computer system in order  
8 to reduce the total power being consumed by the computer system.

1           2.       The system of Claim 1 further comprising a static power management system  
2 wherein power is withdrawn from components that are not currently active to reduce the power  
3 consumption of the computer system.

1           3.       The system of Claim 2, wherein the static power management system further  
2 comprises a circuit for disconnecting the address, control data in and data out pins of a  
3 component of the computer system in order to reduce the power consumption of the computer  
4 system.

1           4.       The system of Claim 1, wherein the clock generator circuit further comprises a  
2 first oscillator that generates a first clock signal, a second clock oscillator that generates a second  
3 clock signal, a programmable clock circuit that generates a third clock signal based on the second  
4 clock signal, and a clock select circuit that selects one of the first, second and third clock signal  
5 that is supplied to a portion of the computer system to provide that portion of the computer  
6 system with a predetermined clock signal.

1           5.       The system of Claim 4, wherein the clock select circuit further comprises a clock  
2 state machine for determining the clock state of the computer system at a predetermined time and  
3 a clock policy circuit for generating control signals to the clock select circuit in order to output  
4 the appropriate clock signal.

1           6.       The system of Claim 5, wherein the clock state machine further comprises an idle  
2 state wherein the computer system is waiting for an input, a busy state wherein the computer

3 system is performing a task, a sleep state wherein the computer system has timed out due to  
4 inactivity and a dead state wherein power has failed to the computer system.

1 7. The system of Claim 6, wherein the clock select circuit further comprises a circuit  
2 that generates a system clock, a circuit that generates a processor clock and a circuit that  
3 generates a co-processor clock wherein each of the clocks is independently and simultaneously.

1 8. The system of Claim 6, wherein, during the idle state, the clock select circuit  
2 generates no clock for the phase locked loop and co-processor so that they are off, the clock  
3 select circuit generates the first clock signal for the processor so that the processor is clocked at a  
4 slow rate and the clock select circuit generates a high rate clock for an interrupt circuit so that the  
5 interrupt circuit is active and can increase the clock frequency for the computer system quickly.

1 9. The system of Claim 6, wherein, during the busy state, the clock select circuit  
2 generates a high rate clock signal for the processor, the co-processor and the interrupt circuits.

1 10. The system of Claim 6, wherein, during the sleep state, the clock select circuit  
2 generates no clock signal for the processor and the co-processor.

1 11. The system of Claim 5, wherein the clock state machine is controlled by an  
2 interrupt signal and software commands.

1 12. The system of Claim 4, wherein the programmable clock circuit generates a fourth  
2 clock signal.

1 13. The system of Claim 12, wherein the first, second, third and fourth clock signals  
2 have different frequencies.

1 14. The system of Claim 13, wherein the first clock signal frequency comprises 32  
2 kHz, the second clock signal frequency comprises 24 MhZ, the third clock signal frequency  
3 comprises 33 MhZ and the fourth clock signal frequency comprises 66 MhZ.

1 15. The system of Claim 4 further comprises a time of day circuit that generates time  
2 of day clock signals based on the first clock signal.

1           16.     The system of Claim 4, wherein the clock select circuit further comprises means  
2     for dynamically changing the clock frequency applied to each component of the computer system  
3     based on the task being performed by the computer system.

1           17.     The system of Claim 4, wherein the clock select circuit comprises a multiplexer.

1           18.     The system of Claim 4, wherein the programmable clock generator further  
2     comprises a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop  
3     that generates a third clock signal and a fourth clock signal having different frequencies.

1           19.     A power management method for a computer system having one or more different  
2     components wherein power is dynamically supplied to each component, the power management  
3     method comprising:

4                 simultaneously generating one or more different clock signals wherein each clock signal  
5     has a different predetermined frequency;

6                 dynamically adjusts the clock signal supplied to each component of the computer system  
7     in order to reduce the total power being consumed by the computer system.

1           20.     The method of Claim 19 further comprising static power management method  
2     wherein power is withdrawn from components that are not currently active to reduce the power  
3     consumption of the computer method.

1           21.     The method of Claim 20, wherein the static power management further comprises  
2     disconnecting the address, control data in and data out pins of a component of the computer  
3     method in order to reduce the power consumption of the computer method.

1           22.     The method of Claim 19, wherein the clock generation further comprises  
2     generating a first clock signal with a first oscillator, generating a second clock signal using a  
3     second oscillator, generating a third clock signal based on the second clock signal, and selecting  
4     one of the first, second and third clock signal that is supplied to a portion of the computer system  
5     to provide that portion of the computer system with a predetermined clock signal.

1           23.     The method of Claim 22, wherein the clock select further comprises determining  
2     the clock state of the computer system at a predetermined time and generating control signals to  
3     the clock select in order to output the appropriate clock signal.

1           24.     The method of Claim 23, wherein the clock state machine further comprises an  
2 idle state wherein the computer method is waiting for an input, a busy state wherein the computer  
3 method is performing a task, a sleep state wherein the computer system has timed out due to  
4 inactivity and a dead state wherein power has failed to the computer system.

1           25.     The method of Claim 24, wherein the clock select circuit further comprises  
2 generating a system clock, generating a processor clock and generating a co-processor clock  
3 wherein each of the clocks is independently and simultaneously.

1           26.     The method of Claim 24, during the idle state, generating no clock for the phase  
2 locked loop and co-processor so that they are off, generating the first clock signal for the  
3 processor so that the processor is clocked at a slow rate and generating a high rate clock for an  
4 interrupt circuit so that the interrupt circuit is active and can increase the clock frequency for the  
5 computer method quickly.

1           27.     The method of Claim 24, during the busy state, generating a high rate clock signal  
2 for the processor, the co-processor and the interrupt circuits.

1           28.     The method of Claim 24, during the sleep state, generating no clock signal for the  
2 processor and the co-processor.

1           29.     The method of Claim 23, wherein the clock state machine is controlled by an  
2 interrupt signal and software commands.

1           30.     The method of Claim 22 further comprising generating a fourth clock signal.

1           31.     The method of Claim 30, wherein the first, second, third and fourth clock signals  
2 have different frequencies.

1           32.     The method of Claim 31, wherein the first clock signal frequency comprises 32  
2 kHz, the second clock signal frequency comprises 24 MhZ, the third clock signal frequency  
3 comprises 33 MhZ and the fourth clock signal frequency comprises 66 MhZ.

1           33.     The method of Claim 22 further comprises a time of day circuit that generates  
2 time of day clock signals based on the first clock signal.

1           34.     The method of Claim 22, wherein the clock select circuit further comprises means  
2 for dynamically changing the clock frequency applied to each component of the computer  
3 method based on the task being performed by the computer method.

1 35. The method of Claim 22, wherein the clock select circuit comprises a multiplexer.

1 36. The method of Claim 22, wherein the programmable clock method further  
2 comprises a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop  
3 that generates a third clock signal and a fourth clock signal having different frequencies.

1 37. A flexible clock generator, comprising:

2 a first oscillator that generates a first clock signal;

3 a second clock oscillator that generates a second clock signal;

4 a programmable clock circuit that generates a third clock signal based on the second  
5 clock signal; and

6 a clock select circuit that selects one of the first, second and third clock signal that is  
7 supplied to a portion of the computer system to provide that portion of the computer system with  
8 a predetermined clock signal.

1 38. The generator of Claim 37, wherein the clock select circuit further comprises a  
2 clock state machine for determining the clock state of the computer system at a predetermined  
3 time and a clock policy circuit for generating control signals to the clock select circuit in order to  
4 output the appropriate clock signal.

1 39. The generator of Claim 38, wherein the clock state machine further comprises an  
2 idle state wherein the computer system is waiting for an input, a busy state wherein the computer  
3 system is performing a task, a sleep state wherein the computer system has timed out due to  
4 inactivity and a dead state wherein power has failed to the computer system.

1 40. The generator of Claim 39, wherein the clock select circuit further comprises a  
2 circuit that generates a system clock, a circuit that generates a processor clock and a circuit that  
3 generates a co-processor clock wherein each of the clocks is independently and simultaneously.

1 41. The generator of Claim 39, wherein, during the idle state, the clock select circuit  
2 generates no clock for the phase locked loop and co-processor so that they are off, the clock  
3 select circuit generates the first clock signal for the processor so that the processor is clocked at a  
4 slow rate and the clock select circuit generates a high rate clock for an interrupt circuit so that the  
5 interrupt circuit is active and can increase the clock frequency for the computer system quickly.

1           42.     The generator of Claim 39, wherein, during the busy state, the clock select circuit  
2 generates a high rate clock signal for the processor, the co-processor and the interrupt circuits.

1           43.     The generator of Claim 39, wherein, during the sleep state, the clock select circuit  
2 generates no clock signal for the processor and the co-processor.

1           44.     The generator of Claim 38, wherein the clock state machine is controlled by an  
2 interrupt signal and software commands.

1           45.     The generator of Claim 37, wherein the programmable clock circuit generates a  
2 fourth clock signal.

1           46.     The generator of Claim 45, wherein the first, second, third and fourth clock  
2 signals have different frequencies.

1           47.     The generator of Claim 46, wherein the first clock signal frequency comprises 32  
2 kHz, the second clock signal frequency comprises 24 MhZ, the third clock signal frequency  
3 comprises 33 MhZ and the fourth clock signal frequency comprises 66 MhZ.

1           48.     The generator of Claim 37 further comprises a time of day circuit that generates  
2 time of day clock signals based on the first clock signal.

1           49.     The generator of Claim 37, wherein the clock select circuit further comprises  
2 means for dynamically changing the clock frequency applied to each component of the computer  
3 system based on the task being performed by the computer system.

1           50.     The generator of Claim 37, wherein the clock select circuit comprises a  
2 multiplexer.

1           51.     The generator of Claim 37, wherein the programmable clock generator further  
2 comprises a prescalar unit and a post scalar unit whose outputs are fed into a phase locked loop  
3 that generates a third clock signal and a fourth clock signal having different frequencies.